VLSI Design Tools & Technology (VDTT) Programme

Dated: 02.05.2018

Short-listing Criteria in the M. Tech programme of VLSI Design Tools and Technology (JVL).

The Programme Executive Committee (PEC) of the VDTT programme met on 1st May 2018 at 1.00 PM for short listing of M. Tech (VDTT) applications.

The following short listing criteria were decided over and above the minimum eligibility condition as laid out in the prospectus.

i) Direct admission (Full time with GATE): Nil

ii) Call for interview (Full time with GATE):

GATE Discipline	Category	Minimum GATE Score	Minimum degree performance
EC	GE/OBC (NCL)	775	60% or 6 CGPA on 10 point scale
	SC/ST/PH	725	55% or 5.5 CGPA on 10 point scale
EE	GE/OBC (NCL)	800	60% or 6 CGPA on 10 point scale
	SC/ST/PH	750	55% or 5.5 CGPA on 10 point scale
CS	GE/OBC (NCL)	630	60% or 6 CGPA on 10 point scale
	SC/ST/PH	580	55% or 5.5 CGPA on 10 point scale
IN	GE/OBC (NCL)	770	60% or 6 CGPA on 10 point scale
	SC/ST/PH	720	55% or 5.5 CGPA on 10 point scale
Others	GE/OBC (NCL)	850	60% or 6 CGPA on 10 point scale
	SC/ST/PH	800	55% or 5.5 CGPA on 10 point scale
IIT B.Tech.	-		CGPA ≥ 8 (GATE score not required)

NOTE:

A. Centrally Funded Technical Institutes other than the IITs are not exempt from the requirement of a GATE score for the full time programme.

B. If you have applied to the programme, and if you meet the shortlisting criteria you may appear for the interview even if you have not received a call letter. However, please bring your transcripts with you.

ii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time)**

A. Candidates should be an employee of a sponsoring company with a confirmation of sponsorship from the sponsor required for being called for the interview.

B. He/She should have a minimum of 1 year experience in research or development

C. He/she should have a minimum 60% or 6 CGPA on a scale of 10 in the qualifying degree

No. of candidates shortlisted: Five

The candidates will be interviewed by the PEC on May 21st (Monday) 2018, followed by an interview of the shortlisted candidates with the sponsoring industries on May 22nd (Tuesday) 2018.

(Prof. Jayadeva)
Coordinator, VDTT Programme

✓ **Dean (Academics)**

Copy to PEC members