

VLSI Design Tools & Technology (VDTT) Programme

Dated: 02.06.2020

Sub: Minutes of VDTT PEC Meeting held on June 2 2020 at 3.30 PM online through MS-Teams.

Short-listing Criteria in the M. Tech and MS-R programme of VLSI Design Tools and Technology (JVL).

The Programme Executive Committee (PEC) of the VDTT programme met on June 2 2020 at 3.30 PM for short listing of M. Tech and MS-R (VDTT) applications.

VDTT is a fully sponsored programme, and the sponsors will have to interview the candidates. As such direct admission through GATE score does not apply to the VDTT programme.

The following short listing criteria were decided over and above the minimum eligibility condition as laid out in the prospectus. The shortlisting criteria and admission procedure are identical for the M.Tech and MS-R programmes.

i) **Direct admission (Full time with GATE): Nil**

ii) **Call for interview (Full time with GATE):**

GATE Discipline	Minimum GATE Score		Minimum degree performance
	GE, OBC, GEN-EWS	SC, ST, PwD	
EC	900	850	Minimum 6.0 CGPA or 60% for GE/OBC/EWS, 5.5 CGPA or 55% for SC/ST/PwD
EE	940	890	
CS	800	700	
IN	940	890	
Others	940	890	
IIT B.Tech.	-	-	CGPA >= 8

No full time MS-R were shortlisted, based on the above shortlisting criteria.

iii) **Call for interview for Full-Time sponsored, Part-Time Regular & Part-Time Industry sponsored candidates (Part-time)**

A. Candidates should be an employee of a sponsoring company **with a signed MoU with the VDTT programme, or a written commitment to the effect that a MoU would be signed in due course.**

B. He/She should have a minimum of 1 year experience

C. He/she should have a minimum 85% or 8.5 CGPA in UG.

No. of candidates shortlisted six (5 part-time MTech, 1 part-time MSR).

The candidates will be interviewed by the sponsoring industries on June 4-5-6 2020, followed by an interview of the shortlisted candidates with IITD faculty on June 7 2020.



(Prof. Shouri Chatterjee)
Coordinator, VDTT Programme



Dean (Academics)

Copy to PEC members

